A1 CONCLD.

logic operation circuit, simultaneously with the gate insulating films of said select transistors; and

forming gate electrodes of the transistors of said peripheral circuit simultaneously with the gate electrodes of said select transistors.

Please add the following new claim 13:

A2

13. (New) The method of manufacturing a semiconductor memory device according to claim 1, wherein said control gate comprises polysilicon.

REMARKS

Claims 1-6 and 13 are all of the claims pending in the present Application. Non-elected claims 7-12 are canceled above. New claim 13 is added. Claims 1-6 stand rejected under 35 USC §102(b) as being anticipated by US Patent No. 5,683,923 to Shimizu et al.

This rejection is respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

As disclosed and claimed, the present invention is directed to a semiconductor memory device capable of electrically writing and erasing data. The device includes a plurality of cell transistors for storing data, each cell transistor having a floating gate electrode and a control gate electrode, and a plurality of select transistors for controlling and selecting the cell transistors. Before the control gate electrodes of the cell transistors are formed, the surface of a substrate directly above channel regions of the select transistors fabricated in the same process as the cell transistors is exposed, and gate

insulating films of the select transistors are formed on the exposed surface of the substrate. The control gate electrodes of the cell transistors are formed, and gate electrodes of the select transistors are formed on the gate insulating films.

The advantage of the present invention is that the number of fabrication steps is reduced.

II. THE PRIOR ART REJECTION

The Examiner asserts that US Patent 5,683,923 to Shimizu et al. anticipates the invention as described by claims 1-6. However, a key feature of the present invention is that the memory cell transistors have a floating gate structure and a corresponding set of switching transistors are fabricated in a partially-concurrent sequence that reduces the number of steps compared to the prior art.

An important part of this sequence is that the two types are fabricated identically until prior to forming the control gate of the cell transistor, at which time the select transistor gate structures are stripped back to the substrate and rebuilt according to their requirements as differing from the cell transistors.

Applicant has been unable to find any reference in the Shimizu reference concerning the fabrication of the select transistors. Shimizu seems only concerned with twelve embodiments of the flash cell structures and totally ignores the switching transistor fabrication. By such silence, Shimizu is interpreted as implying that the switching transistors are separately fabricated. Indeed, line 31 of column 3 suggests that the Shimizu configuration does not use the select transistors. If the Examiner wishes to maintain the rejection based on Shimizu, Applicant respectfully requests that the select transistor fabrication sequence be specifically identified in Shimizu by column and line number.

Moreover, even assuming the Examiner is referring to the embodiment of Figures 1 and 2, as indicated in the rejection, the rejection seems to refer to the cell transistor as also being at least part of the select transistor. Applicant is unable to find any reference in the description that these figures refer to anything except the cell transistors. If the Examiner wishes to maintain this rejection based on Shimizu, Applicant respectfully

requests that the select transistor components be specifically identified in the figures.

Hence, turning to the clear language of the claims, there is no teaching or suggestion of "... before forming the control gate electrodes of said cell transistors, exposing a surface of a substrate directly above channel regions of said select transistors fabricated in the same process as the cell transistors ...."

Additionally, if it is assumed in the Shimizu technique that the select cell transistors and the flash cell structures are fabricated simultaneously, the trenches are formed in a region of a cell transistor and a region of a select transistor shown in Figures 33 and 34, and a floating gate electrode and a control gate electrode are formed in the trenches shown in Figure 35. Because a floating gate electrode is unnecessary for the select transistor, the polysilicon for a floating gate electrode would have to be removed from a region of a select transistor before forming the control gate electrode. However, because a polysilicon for a floating gate electrode is left at the wall inside the trench, it is very difficult to remove it completely. Therefore, using the method of Shimizu, it would be difficult to form a select transistor where only a polysilicon for the control gate electrode is embedded inside the trench, as emphasized by new claim 13.

For these reasons, the claimed invention is fully patentable over the Shimizu reference.

Further, the other prior art of record has been reviewed, but it too even in combination with Shimizu fails to teach or suggest the claimed invention.

III. Formal matters and Conclusion

Applicant submits that claims 1-6 and 13, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 4/12/02

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 7-12 have been canceled.

Claims 1-4 are revised as follows:

1. (Amended) A method of manufacturing a semiconductor memory device capable of electrically writing and erasing data, said semiconductor memory device having a plurality of cell transistors for storing data, each of said cell transistors having a floating gate electrode and a control gate electrode, and a plurality of select transistors for controlling and selecting said cell transistors, said method comprising [the steps of]:

before forming the control gate electrodes of said cell transistors, exposing a surface of a substrate directly above channel regions of said select transistors fabricated in the same process as the cell transistors;

forming gate insulating films of said select transistors on the exposed surface of the substrate; and

forming the control gate electrodes of said cell transistors and forming gate electrodes of said [cell transistors and forming gate electrodes of said] select transistors on said gate insulating films.

2. (Amended) The method of manufacturing a semiconductor memory device according to claim 1, further comprising [the step of]:

simultaneously forming a first diffused layer serving as source and drain regions of said cell transistors and a second diffused layer serving as source and drain regions of said select transistors.

3. (Amended) The method of manufacturing a semiconductor memory device according to claim 1, further comprising [the steps of]:

forming gate insulating films of transistors of a peripheral circuit comprising a logic operation circuit, simultaneously with the gate insulating films of said select transistors; and

forming gate electrodes of the transistors of said peripheral circuit simultaneously with the gate electrodes of said select transistors.

4. (Amended) The method of manufacturing a semiconductor memory device according to claim 2, further comprising [the steps of]:

forming gate insulating films of transistors of a peripheral circuit comprising a logic operation circuit, simultaneously with the gate insulating films of said select transistors; and

forming gate electrodes of the transistors of said peripheral circuit simultaneously with the gate electrodes of said select transistors.

New claim 13 has been added, as follows:

13. (New) The method of manufacturing a semiconductor memory device according to claim 1, wherein said control gate comprises polysilicon.